REMARKS

The Office Action states that the amendment filed March 28, 2003 includes new matter under 35 USC 132. Specifically, the Office Action states that the original disclosure fails to support the language added to claims 1-5 and 15-19 directed to "including an integrated circuit," and the terms "first terminal" connected to an "amplifier" and the "second terminal" connect to an "amplifier" or "an output of a signal source" recited in claims 4, 5, 12-14, 18-23 and 26-28. The rejection is respectfully traversed.

The invention specifies the injection-nulling switch, which covers the switch element itself (Fig. 5 and Fig. 6). The switch element is connected to form the integrated circuit, as in Fig. 7d, together with an amplifier. The switch elements are made up of MOS transistors, which are integrated circuits by nature. The invention (Fig. 5 and Fig. 6) gives a generic form that can be implemented using different type of MOS transistors (as in Fig. 7d). Hence, the drawings fully disclose the claimed subject matter. In any event, the term "integrated circuit" has been removed from the claims. No new matter has therefore been added.

Claims 1-5 and 15-19 have been objected to as using the terms "including" and "comprising" with respect to the term "circuit." The claims have been amended, as detailed above.

Claims 1-5, 12-23 and 26-28 have been rejected under 35 USC 112, first paragraph, and claims 1-5, 12-20 and 26-28 have been rejected under 35 USC 112, second paragraph. Specifically, the Examiner has rejected the claims for use of the term "integrated circuit." This term has been removed from the claims.

The rejection to claims 1-9, 12-14 and 27-28 has been maintained under 35 USC 102(b) as anticipated by Hirano. The rejection is respectfully traversed.

Hirano discloses a semiconductor device provided with a charge-discharge capacitor and a plurality of charge collection capacitors which are respectively connected in parallel to the charge-discharge capacitor via switches. Referring, for example, to Figure 1 of Hirano, it is clear that switches ST1 and ST2 are connected to a common node N10, which connects to SD1, CR1, SC1,

ST3 and ST4. In the claimed invention, switch S2 is connected to switch S1 at terminal H, and connects to an input of an amplifier that exhibits high impedance. Terminal L connects to an output of a signal source that exhibits low impedance. Additionally, in Hirano, clocking of the switches SC1, ST1, ST2, ST3, ST4 and SD1 occurs by non-overlapping clock signals, whereas, in the claimed invention, clocking of the switches S1 and S2 occurs by two phase-shifted clock signals. Finally, in Hirano, DC charge transfer takes place into the capacitors for the memory-cell-array operation. In the claimed invention, compensation of non-ideal charge injection and clock feed-through error are injected into the capacitor at a high impedance node that is connected to the input of an amplifier that exhibits high impedance.

In response to the arguments presented, the Examiner specifically comments that "the claim language discussed by Applicant does not appear in these claims." Applicants' respectfully disagree. For example, the claims recite "a first switching element coupled to a first terminal and a second terminal." Specifically, switch S2 in the invention is connected to switch S1 at terminal H, and will connect to an input of an amplifier where it exhibits high impedance, whereas terminal L will connect to output of a signal source where it exhibits low impedance. The Examiner also comments that the term "high impedance" is unclear. Again, Applicants' respectfully disagree. Although the term "high impedance" may be a relative term, in this case, it is relative to the circuit being claimed. Therefore, a high impedance is considered that which is "high" for the specific circuit.

Claims 15-23 and 26 would be allowable if rewritten in independent form to overcome the rejections under 35 USC 112, second paragraph. The 112, second paragraph rejections being overcome, claims 15-23 and 26 are in condition for allowance.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant(s) petition(s) for

any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or fees due in connection with this document to **Deposit Account No. 03-1952** referencing docket no. 529002000100.

Dated: October 14, 2003

Respectfully submitted,

By _____

Kevin R. Spivak
Registration No.: 43,148
MORRISON & FOERSTER LLP
1650 Tysons Blvd, Suite 300
McLean, Virginia 22102
Phone (703) 760-7762
Facsimile (703) 760-7777
Attorneys for Applicant